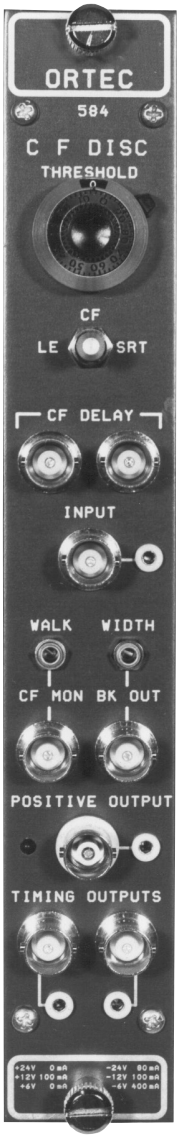
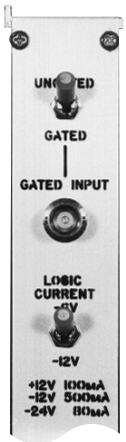
ORTEC®

AMETEK®

584
Constant-Fraction Discriminator

- **Good time resolution over a wide range of pulse amplitudes with scintillation and semiconductor detectors**
- **50-MHz count-rate capability**
- **5 mV minimum threshold**
- **Time walk ≤100 ps for 100:1 dynamic range**
- **Constant-fraction, leading-edge, and slow-rise- time reject modes**





The ORTEC Model 584 Constant-Fraction Discriminator allows good time resolution to be obtained from all commonly used detectors such as HPGe, silicon charged-particle, fast plastic, NaI(Tl), and photomultiplier tubes. Three timing modes are provided in the Model 584: constant-fraction, constant-fraction with slow-rise-time reject, and leading-edge. This economical unit has a minimum threshold of –5 mV, allowing good timing measurements to very low energies. The maximum input signal acceptable without saturation is –5 V, which provides a 1000:1 input dynamic range. The Model 584 is useful in high-count-rate applications to 50 MHz with ≤20 ns pulse-pair resolving time. The time walk of the Model 584 is ≤±100 ps for a 100:1 input dynamic range.

A variety of controls is provided, allowing optimization of the Model 584 in various applications. A precision 10-turn potentiometer sets the threshold from –5 mV to –1 V. The blocking time set by the Blocking Output Width is continuously adjustable from ≤10 to ≥1000 ns. This feature is useful for preventing multiple triggering on pulses from scintillators having long decay time, e.g., NaI(Tl). A front-panel LED indicates that the discriminator has been triggered and can therefore be used to set the threshold just above the noise. Walk is adjusted by a front-panel 20-turn potentiometer. The Constant-Fraction Monitor on the front panel can be used to optimize walk adjustment. Since the constant-fraction shaping delay is selected by external cable, the optimum delay for a specific detector application is easily selected.

Four NIM-standard output signals are available from the Model 584. The positive output signal is continuously variable from ≤0.5 to ≥2.5 µs by means of a printed wiring board (PWB) potentiometer. The polarity of the positive output is PWB selectable to be either a NIM-standard positive output signal or the complement signal. The two timing output signals are NIM-standard fast negative logic signals, each having a 2-ns rise time and a 5-ns width FWHM. The blocking output signal is a NIM-standard fast negative logic signal whose width is adjustable from ≤10 to ≥1000 ns.

The Model 584 can be gated externally. A rear-panel locking toggle switch selects either Gated or Ungated operation. In the Gated Mode, a printed wiring board jumper selects the Bin Gate line in the NIM bin, a NIM-standard positive signal via the rear-panel BNC connector, or a NIM-standard negative signal via the rear-panel BNC connector.

Logic current for the Model 584 is selected from either the –6 V or –12 V NIM supply by means of a rear-panel locking toggle switch. The Model 584 is within the allotment of current for a single-width NIM module for a NIM Class V power supply when the logic current is obtained from –6 V.

Specifications

PERFORMANCE

INPUT Accepts negative input signals from 0 V to –5 V without saturation; DC-coupled; Z_{in} = 50 Ω; reflections ≤±5% for t_r ≤2 ns.

THRESHOLD RANGE –5 mV to –1 V.

THRESHOLD INTEGRAL NONLINEARITY ≤±0.25% of full scale.

THRESHOLD INSTABILITY ≤±100 µV/°C, 0 to 50°C.

PROPAGATION DELAY Nominally 25 ns, with external CF Delay ≈2 ns.

MINIMUM PULSE-PAIR RESOLUTION ≤20 ns.

DEAD TIME Nominally 20 ns or Blocking Output Width, whichever is greater.

BLOCKING OUTPUT WIDTH Adjustable from ≤10 to ≥1000 ns.

TIME WALK ≤±100 ps for the 100:1 input range from –20 mV to –2 V. Conditions: External CF Delay = 2 ns; input rise time ≤1 ns; input pulse width = 10 ns.

CONTROLS

THRESHOLD Front-panel 10-turn precision locking potentiometer determines the discriminator threshold setting in the range from –5 mV to –1 V.

TIMING MODE SWITCH Front-panel 3-position locking toggle switch selects one of the three timing modes:

CF (Constant-Fraction) Attenuation factor is internally set at f = 0.2 (can be changed upon request). An external 50-Ω coaxial cable must be provided for the constant-fraction shaping delay (CF Delay).

SRT (Slow-Rise-Time) Reject Provides constant-fraction timing and inhibits output signals that would be produced by leading-edge timing from the leading-edge arming discriminator. An input signal that does not cross the discriminator threshold before the constant-fraction zero-crossing time does not produce an output pulse.

LE (Leading-Edge) Inhibits timing from the constant-fraction circuitry. The timing is derived as the leading edge of the input signal crosses the discriminator threshold level.

CF DELAY Two front-panel BNC connectors accept 50-Ω coaxial cable to set the required constant-fraction shaping delay for the CF and SRT Modes: total delay is ≈0.8 ns plus the delay of the external cable. In the LE Mode, the user may either connect a piece of 50-Ω coaxial cable between these two connectors or connect a 50-Ω termination to each of the two connectors.

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WALK Front-panel 20-turn screwdriver adjustment sets the walk compensation for each application.

CF MON Front-panel BNC connector permits observation of the constant-fraction bipolar timing signal; Z_o = 50 Ω. 50-Ω coaxial cable required; 50-Ω termination suggested.

WIDTH Front-panel 20-turn screwdriver adjustment sets the width of the Blocking Output pulse. Variable from ≤10 to ≥1000 ns. Sets the instrument dead time for widths greater than nominally 20 ns.

GATING MODE SWITCH Rear-panel 2-position locking toggle switch controls the use of the Gate Inputs. (One of three Gate Input signal paths is selected by a PWB jumper.)

Gated A "true" logic level from the selected Gate Input permits output signals to be generated by the discriminator. A "false" logic level from the selected Gate Input inhibits output signals from being generated by the discriminator. A set of Output signals already in progress is not terminated prematurely by a logic "false" signal from the selected Gate Input.

Ungated The signal level of the selected Gate Input does not inhibit normal generation of output signals from the discriminator (i.e., the discriminator is always enabled).

LOGIC CURRENT SWITCH Rear-panel 2-position locking toggle switch selects either the –6 V or the –12 V NIM supply line for providing current for the high-speed ECL logic used in the discriminator.

NOTES:

(1) The module is within the current allotment for a single NIM width when using the –6 V position with a NIM Class V power supply or equivalent.

(2) The module exceeds the current allotment for a single NIM width on the –12 V supply when using the –12 V position. However, this position permits using the discriminator in bins with power supplies not providing –6 V.

GATE INPUT JUMPER (G+, G–, or BG) PWB jumper selects one of three Gate Input signal paths:

G+ Selects the rear-panel BNC Gate Input connector to accept slow positive NIM input signal levels for gating; DC-coupled; Z_{in} >1 kΩ.

G– Selects the rear-panel BNC Gate Input connector to accept fast negative NIM input signal levels for gating; DC-coupled; Z_{in} = 50 Ω.

BG Selects the Bin Gate line (pin 36 of the NIM power connector block) to accept slow positive NIM input signal levels >+2 V for gating; DC-coupled; Z_{in} >1 kΩ.

POSITIVE OUTPUT WIDTH (+ Width) PWB 4-turn potentiometer sets the width of the slow positive NIM output signal in the range from ≤0.5 to ≥2.5 µs.

POSITIVE OUTPUT SIGNAL POLARITY (PO or $\overline{PO}$) PWB jumper selects the slow positive NIM output signal (PO) or the complement output signal ($\overline{PO}$).

INPUTS

INPUT Front-panel BNC connector accepts fast negative input signals from 0 V to –5 V without saturation; DC-coupled; Z_{in} = 50 Ω; reflections ≤±5% for t_r ≥2 ns.

GATE INPUT Rear-panel BNC connector; input signals accepted according to PWB Gate Input Jumper.

G+ Jumper Position Accepts slow positive NIM input signal levels for gating; DC-coupled; Z_{in} >1 kΩ.

G– Jumper Position Accepts fast negative NIM input signal levels for gating; DC-coupled; Z_{in} = 50 Ω.

OUTPUTS

TIMING Two front-panel BNC connectors provide simultaneous NIM-standard fast negative logic signals; t_r ≈2 ns; t_f ≈3 ns; t_w ≈5 ns.

BK OUT Front-panel BNC connector provides a NIM-standard fast negative logic pulse that occurs simultaneously with the Timing Outputs; width variable by front-panel adjustment from ≤10 to ≥1000 ns; t_r ≅2 ns.

POSITIVE Front-panel BNC connector provides NIM-standard slow positive logic pulse simultaneously with Timing Outputs; Z_o <10 Ω; width variable by PWB width adjustment from ≤0.5 to ≥2.5 µs. The associated LED is triggered for approximately 3 ms (updating) by each positive output pulse.

ELECTRICAL AND MECHANICAL

WEIGHT
Net 1.2 kg (2.6 lb).
Shipping 2.25 kg (5.0 lb)

DIMENSIONS NIM-standard single-width module 3.43 X 22.13 cm (1.35 X 8.714 in.) per DOE/ER-0457T.

POWER REQUIRED

Logic Current Switch*

	Position	
	–6 V (mA)	**–12 V (mA)**
+12 V	100	100
–12 V	100	500
+6 V	0	0
– 6 V	400	0
+24 V	0	0
– 24 V	80	80
117 V AC	0	0

*See "NOTES" on Logic Current Switch, "Controls" Section of Specifications.

Ordering Information

Model	Description
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Specifications subject to change
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