

ORTEC®

DSP^{EC} 50/50A and DSP^{EC} 502/502A



Superior Digital Signal Processing Based
Gamma-Ray Spectrometers

AMETEK®
ADVANCED MEASUREMENT TECHNOLOGY

DSP^{EC}50/50A and DSP^{EC}502/502A

Experience-Based Performance

The DSPEC[®] 50 and DSPEC 502 salute the 50th year in which ORTEC has delivered innovative and quality nuclear instrumentation to scientists in a broad range of applications worldwide. Fifteen years after the first ORTEC DSPEC digital spectrometer received acclaim among spectroscopists for its performance and stability, the DSPEC 50 and DSPEC 502 are landmark products which bring together our long design experience in digital spectrometers and the ongoing innovation skills of our developers.¹

The DSPEC 50 and DSPEC 502 are available in the original Standard and newer Advanced models. Both models have the same superior digital signal processing and stability for optimal spectroscopic performance while the Advanced models include features to optimize coincidence timing applications, such as Compton Suppression and Cosmic Veto, Operating System independence through web interfaces, and other enhancements.

Advanced Model Features (DSPEC 50A and DSPEC 502A)

•ADC Conversion Gain up to 64k channels for expanded energy range applications!

•Digital Coincidence Timing for simplified Compton Suppression and Cosmic Veto Systems with excellent performance!

Configurable Output Port Options

Change Sample: Output on software command for Sample Changer operation

CRM: Output on Fast Channel Detect

SCA: Output on Peak Height within ROI during acquisition or continuous

ADC Gate: Output when Gate is active

Configurable Coincidence and Gate Options

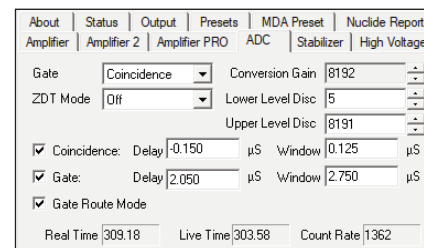
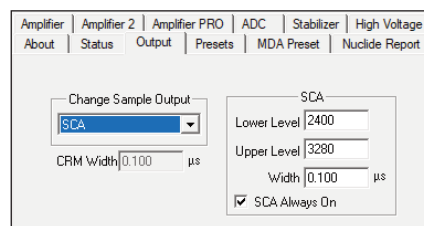
Gate: Same options as standard (Off, Coincidence, and Anticoincidence)

Coincidence Delay and Window: Optimize coincidence between gate input and ADC fast channel.

Gate Delay and Window: Program Gate start and duration for coincidence events.

Gate Route Mode: Coincidence and Anticoincidence data collected concurrently. Both spectra and the total can be saved and recalled with the N42 (2012) spectrum file.

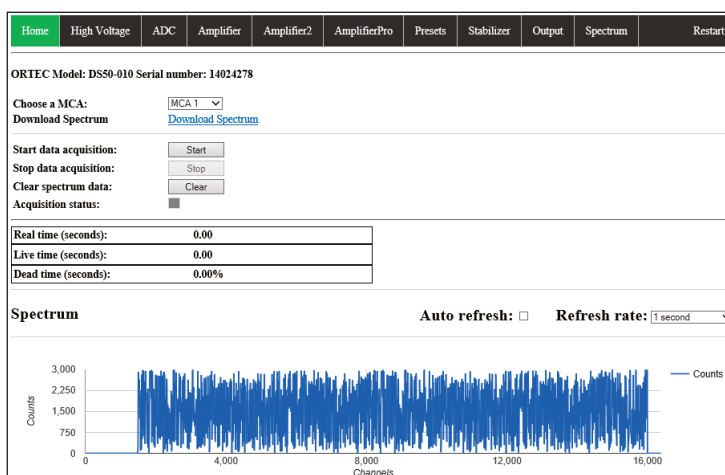
These functions eliminate the need for complex timing electronics configurations that have traditionally been required for coincidence timing systems with excellent performance characteristics. Simply connect the output of the veto detector (i.e. annulus/plug in Compton Suppression or plastic panel in cosmic veto) to the Gate of the High Purity Germanium Detector with the output trigger set to CRM (Fast Channel Detect) and optimize the Coincidence and Gate timing on the HPGe detector. Yes, it is really that simple! And the Gated, Ungated, and Total Spectra can all be saved at the same time in the same XML-based ANSI N42 spectrum file!



•Web Page and Web Services Interfaces for Operating System independence!

The Web Page Interface is hosted directly on the instrument and enables hardware configuration and basic MCA Emulation functions to acquire and save spectra without the need to install any software. Simply enter the Web Address configured on your instrument in your browser to get started. The Web Interface is available with most modern browser applications run on any operating system including Windows, Linux, Android, and Apple systems.

The Web Service is a programming interface hosted on the instrument for custom application development in any operating system and development environment that supports Web Services. No need for any special driver or software installation, and example projects are available on the ORTEC website to help jump start your development.



¹DSPEC 50 refers to all models unless otherwise stated.

DSP^{EC} 50/50A and DSP^{EC} 502/502A

Features Common to Standard and Advanced Models

- Single MCA (DSPEC 50/50A) and dual MCA (DSPEC 502/50A) versions.
- Highly stable against variations in count rate and temperature.
- Automated set-up: Automatic Pole Zero Adjust, Baseline Restorer, and Optimize.²
- Digital spectrum stabilizer.
- USB 2.0 and Ethernet (TCP/IP) connectivity
- High throughput capabilities for high count rate applications.
- Large front panel display for at-a-glance system status information.
- Support for all HPGe detector types, old and new.
- 16k ADC Conversion Gain
- “Loss Free” or “Zero Dead Time” (ZDT)³



The usual way to account for counting losses at high rates is by extending the acquisition time. The underlying assumption is that the sample count rate does not change during the total counting period. This is far from true when short half lives are encountered or the sample is in motion (e.g., flowing through a pipe). ORTEC has refined the loss-free counting technique in the digital domain. In this method, the spectrum itself is corrected pulse by pulse, and the ZDT method provides both an accurately corrected spectrum and correctly calculated statistical uncertainty.

• “Enhanced Throughput” Mode

Accuracy at high input count-rates can be limited by the speed at which the spectrometer stores data to memory. It is said to be “throughput-limited.” Pulse pileup means that beyond a certain point, as input count-rate increases still further, the rate of data stored to memory DECREASES, reducing result quality. By developing a new kind of digital peak detection algorithm, ORTEC has increased the maximum throughput by up to 30% by removing some of the dead time associated with the process of pulse peak amplitude determination.

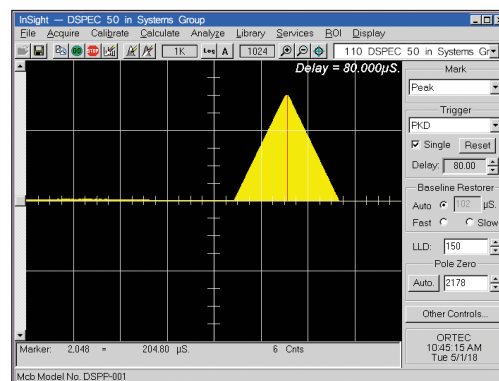
• List Mode

For situations in which the sample is moving relative to the detector, it is often vitally important to be able to measure an activity profile as a function of time. Examples of such applications include aerial and land-based surveying and portal monitoring. It is usually a requirement that no “dead periods” occur, associated with the acquire-store-clear-restart cycle. In the list mode of operation, data are streamed directly to the computer, event by event. There is no associated “dead period.” In the DSPEC 50 implementation, each event is timestamped to an accuracy of 200 nanoseconds.

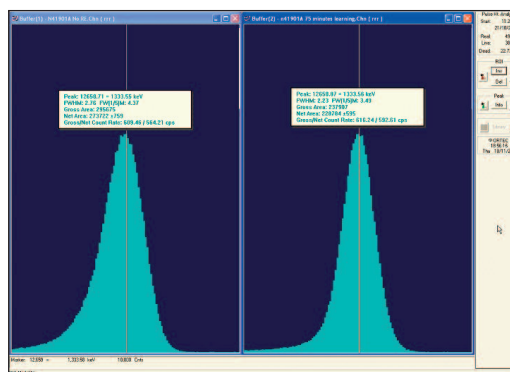
• Ballistic Deficit and Charge Trapping Correction

The trapezoidal digital filter in the DSPEC 50 is the same as all other ORTEC DSPEC family members. It allows adjustment of the filter to optimize the resolution performance of large HPGe detectors which often have low-side peak tailing when ballistic deficit is present. These large detectors are increasing in use in low level counting applications. The adjustment is largely automated by the use of the “OPTIMIZE” feature and may be monitored by the InSight™ Virtual Oscilloscope mode.

The DSPEC 50 offers even further capability in the form of the Resolution Enhancer, a charge trapping corrector which can be used to reduce the peak degradation for neutron damaged detectors. The neutron damage to the crystal lattice causes “trapping” centers which hold some of the charge created by the gamma-ray interaction. This results in low-side tailing similar to ballistic deficit although the cause is different. The charge trapping corrector is calibrated or “trained” for the individual detector such that it adds back the pulse height deficit, event by event.



InSight Virtual Oscilloscope Mode.



The charge trapping corrector improves FWHM resolution by 20% on an N-type detector.

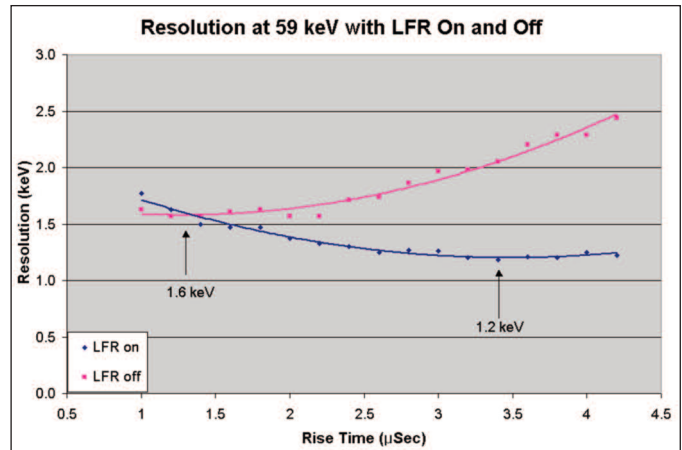
²Patent No. 5,872,363

³Patent No. 6,327,549

DSP^{EC}50/50A and DSP^{EC}502/502A

•Low-Frequency Rejector (LFR)

HPGe detectors do not always perform well in environments where there is mechanical vibration. Microphonic noise degrades energy resolution by adding low frequency periodic electrical noise to the primary signal. Electrical ground loops are also a source of low frequency electrical noise. The increasing use of mechanical coolers for HPGe detectors to eliminate the need for LN2 and increasing need to take HPGe detectors out of the laboratory environment mean an increase in mechanical vibration. DSPEC 50 incorporates a Low-Frequency Rejector (LFR) Filter feature, which reduces the effects of such noise sources.



The effect of the LFR filter on a mechanically cooled HPGe detector.

DSPEC 50 Display Modes

The large color display of the DSPEC 50 is used in the initial set-up of the Ethernet communications. The status displays can be used to provide several standard views:

•The “Gauges Display”

The gauges display provides a simple-to-read analog representation of the system acquisition status, the green background indicates “count in progress”.

•The “Big Numbers” Display

The big numbers display provides status information clearly visible from a distance.

•The “Chart” Display

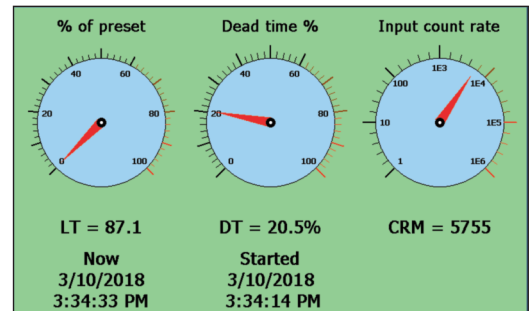
The chart display monitors count-rate, dead time, and gain stabilizer activity during acquisition, thereby providing reassurance that all is well. The gain stabilizer display is only shown when the gain stabilizer is enabled.

•Spectrum Display

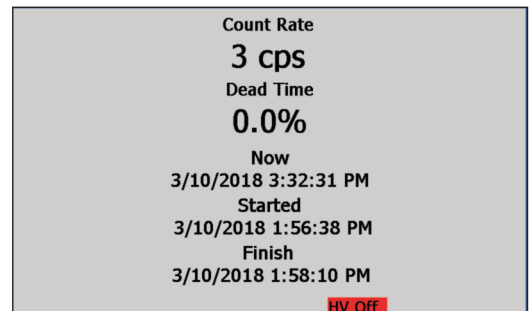
The spectrum display provides a live spectral display which will show all ROIs set in the unit. In addition, ROIs may be set for the net area which can be used to perform a simple activity estimate based on the net area, the live time, and a user supplied factor (yellow). This permits the display of on-screen activity estimates for acquiring peaks.

•Displays Set-Up Screen

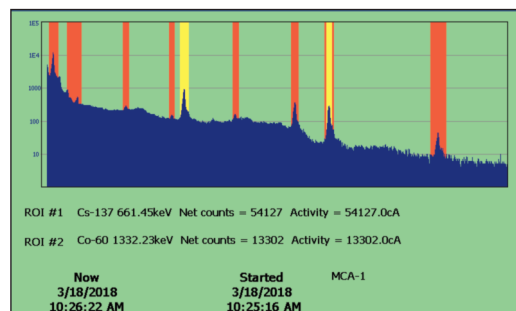
A simple to use displays set-up screen allows a user to choose what is displayed and the duration of the display type if more than one is chosen. User supplied JPGs may also be displayed.



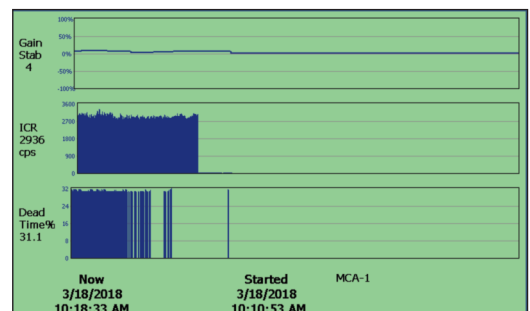
The “Gauges” Display.



The “Big Numbers” Display.



The “Spectrum” Display.



The “Chart” Display.

DSP^{EC}50/50A and DSP^{EC}502/502A

Instrument Control via Software

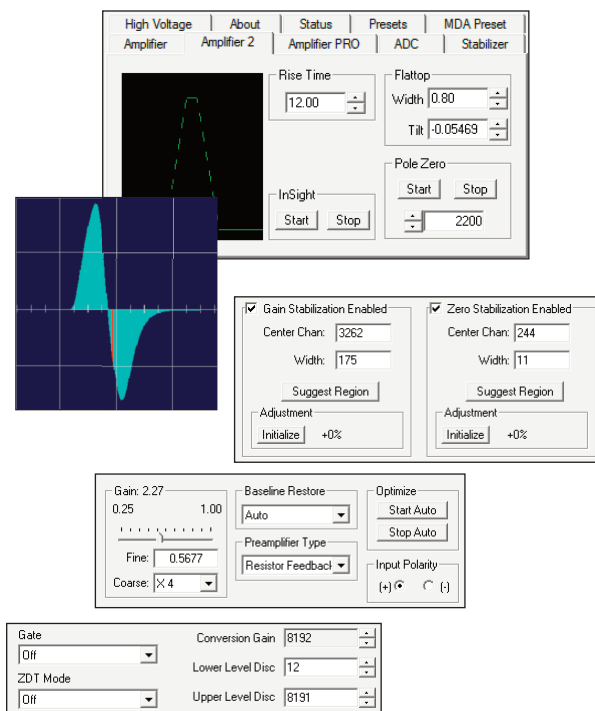
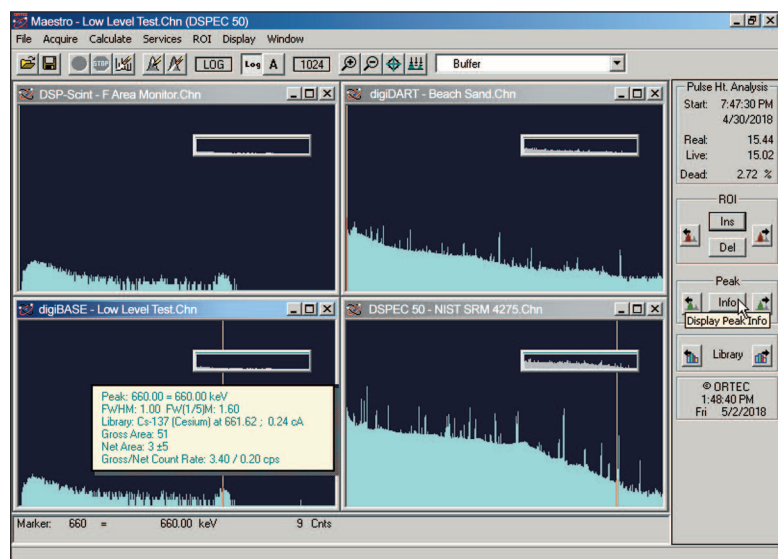
The DSPEC-50 is entirely software controlled and can be configured and operated using a variety of ORTEC software applications such as MAESTRO, MAESTRO-Pro, and GammaVision, as well as the CONNECTIONS Programmer's Toolkit. The Advanced model can also be setup and controlled using the Web Page or Web Services without having to install additional software.

The Standard models (DSPEC-50/502) include a single user license of the traditional MAESTRO MCA Emulation software for a simple setup and data acquisition experience. The Advanced models (DSPEC-50A/502A) include a single user license of MAESTRO-Pro which has more extensive functionality, including support for the new instrument features.

MAESTRO-Pro vs. MAESTRO

| Feature | MAESTRO | MAESTRO-Pro |
|--|--|--|
| Languages | English | English, German, Chinese, French, Russian |
| Spectrum File Formats | CHN, SPC, SPE | CHN, SPC, SPE, N42 (2006 and 2012) |
| DSPEC-50A/502A Gate Route Mode Support | No | Yes |
| 32k and 64k Channel Spectrum Support | No | Yes |
| Calibration Features | Basic Energy Calibration | Automated and Interactive Energy, FWHM, and Efficiency with Calibration Reports and Graphical Display |
| Peak Fit | Basic Region of Interest (ROI) | Basic Region of Interest (ROI), Interactive Peak Fit with multiplets, Display Peak Fit from GammaVision analysis |
| Automation Functions | Basic spectrum acquisition and ROI reporting functions | Comprehensive automation from GammaVision with the exception of spectrum analysis |
| Library Editor | External Library Editor | Internal Editor compatible with Nuclide Navigator when installed |
| Security | None | Menu Passwords |
| External Spectrum Viewer | WinPlot | GVPlot |

Refer to the MAESTRO and MAESTRO-Pro literature for additional information.



DSP^{EC}50/50A and DSP^{EC}502/502A

Advanced Model Specifications (DSPEC 50A/502A)

System Conversion Gain: 256 to 64k channels.

Digital TTL Counters: Via Sample Ready and Gate Ports synchronized with spectrum acquisition.

Web Page and Web Services Interface: For basic MCA Emulation, hardware configuration and programming.

Configurable TTL Output Port (Change Sample Port):

- Change Sample command with user-defined pulse width
- Input Count Rate based on fast channel trigger
- SCA Count Rate for each pulse in a region of interest
- ADC Gate based on Coincidence and Gate logic

Configurable Coincidence and Gate

- Coincidence Logic: Gate TTL pulse compared to internal fast channel with adjustable offset and window (25 nS increments up to $\pm 6.375 \mu\text{S}$).
- Gate Window: Defined by delay after coincidence detection and gate width to cover peak detection (25 nS increments up to 200 μS).
- Gate Route Mode: All events saved as gated or not gated in separate memory. The Gated, Ungated, and Total spectrum can be saved to a common N42 (2012) spectrum format and read individually using GammaVision and other applications compatible with N42 (2012) files.

Specifications Common to Standard and Advanced Models

Display: 7" backlit color LCD provides status information. Displayed information is selectable by the user.

USB 2.0 Connection: For use when connecting one or more DSPEC 50 or 502 instruments to a single computer. ORTEC CONNECTIONS software supports up to 255 USB-connected devices per computer.

Ethernet Connection: Allows control of a DSPEC 50 from one or more PCs across a network. Standard 10/100M Ethernet connection. TCP/IP Protocol. Link and Activity LEDs are integrated into the RJ-45 connector.

System Gain Settings:

Coarse Gain: 1, 2, 4, 8, 16, 32, 64, and 128.

Fine Gain: 0.5 to 1.1.

The available range of gain settings supports all types of HPGe detectors. Specifically, the following maximum energy values are achievable using the standard ORTEC preamplifier (maximum gain to minimum gain):

| | |
|---------|-------------------|
| COAX | 187 keV to 24 MeV |
| LO-AX | 94 keV to 12 MeV |
| GLP/SLP | 16.5 keV to 2 MeV |
| IGLET-X | 8 keV to 1 MeV |

Preamplifiers: Computer selectable as either resistive or TRP preamplifier.

System Conversion Gain: 512 to 16k channels.

Digital Filter Shaping-Time Constants:

Rise Times: 0.8 μs to 23 μs in steps of 0.2 μs .

Flat Tops: 0.3 to 2.4 in steps of 0.1 μs .

Digital Spectrum Stabilizer: Controlled via computer, stabilizes gain and zero errors.

System Temperature Coefficient

Gain: $< 50 \text{ ppm}/^\circ\text{C}$. [Typically $< 30 \text{ ppm}/^\circ\text{C}$.]

Offset: $< 5 \text{ ppm}/^\circ\text{C}$ of full scale, with Rise and Fall times of 12 μs , and Flat Top of 0.8 μs . (Similar to analog 6 μs shaping.)

Maximum System Throughput: $> 100,000 \text{ cps}$ with LFR off. $> 34,000 \text{ cps}$ with LFR on. Depends on shaping parameters.

Pulse Pile-Up Rejecter: Automatically set threshold. Pulse-Pair Resolution: Typically $< 500 \text{ ns}$.

Automatic Digital Pole-Zero Adjustment: Computer controlled. Can be set automatically or manually. Remote diagnostics via InSight Oscilloscope mode. (Patented.)

Digital Gated Baseline Restorer: Computer controlled adjustment of the restorer rate (High, Low, and Auto). (Patented.)

LLD: Digital lower level discriminator set in channels. Hard cutoff of data in channels below the LLD setting.

ULD: Digital upper level discriminator set in channels. Hard cutoff of data in channels above the ULD setting.

Ratemeter: Count-rate display on MCA and/or PC screen.

Battery: Internal battery-backed up memory to maintain settings in the event of a power interruption.

Inputs and Outputs

If both MCAs are installed (502 model), each MCA has each of the following connectors:

Detector: Multipin connector (13W3) with the following:

Preamp Power: 1 W maximum (+12 V, -12 V, +24 V, -24 V, 2 GND).

Analog In: Normal amplifier input.

TRP Inhibit.

Power for SMART-1 or DIM.

Control of HV and SMART-1 Detector (2 wires).

Analog In: Rear-panel BNC accepts preamplifier signals of either polarity, with rise times less than the selected Flat Top Time setting and exponential decay time constant in the range of 40 μs to infinity (including transistor-reset and pulsed-optical reset preamplifiers). Input impedance $> 500 \Omega$, input is dc-coupled and protected to $\pm 12 \text{ V}$.

ADC Gate In: Rear-panel BNC accepts slow positive NIM input; computer selectable as off, coincidence, or anticoincidence. ADC GATE must overlap and precede the Flat Top region by 0.5 μs , and extend beyond the Flat Top region by 0.5 μs . InSight Oscilloscope allows easy alignment of the ADC GATE signal with the digital output pulse.



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Inhibit In: Rear-panel BNC connector accepts reset signals from transistor-reset (TRP) or pulsed-optical (POF) preamplifiers. Positive NIM logic or TTL level can be used. Inhibit input initiates the protection against distortions caused by preamplifier reset. This includes turning off the baseline restorer, monitoring the overload recovery, and generating the pile-up reject and busy signals for the duration of the overload. These last two signals are used internally to provide information to the dead-time correction circuitry.

USB 2.0: Universal serial bus for PC communications.

Ethernet Connection: Standard 10/100M Ethernet connection. Link and Activity LEDs are integrated into the connector.

Electrical and Mechanical

Change Sample Out: Rear panel BNC connector, TTL compatible.

Sample Ready In: Rear-panel BNC connector, accepts TTL level signal from Sample Changer. Software selectable polarity.

Preamp Power Out: Rear-panel, 9-pin D connector; provides ± 24 V and ± 12 V for preamplifier power.

Dimensions: 42.55 cm W x 35.56 cm D x 15.24 cm H (16.75 in. W x 14 in. D x 6 in. H).

Weight

DSPEC 50: 11 kg (24.25 lbs).

DSPEC 502: 11.7 kg (25.8 lbs).

Power

Input Voltage: 100–220 V AC.

Input Frequency: 47–63 Hz.
110 watts.

Operating Environment: 0° to 50°C. Humidity: 0 to 95%, non-condensing.

Operating Systems: Windows 10, 8.1 and 7 via CONNECTIONS.

CE: Conforms to CE standards for radiated and conducted emissions, susceptibility and low-voltage power directives.

NRTL: Certification verifies, through OSHA-approved NRTL certification authority TÜV SÜD, that the product meets U.S. electrical safety standards (UL/ANSI).

HPGe Detector High Voltage Supplies

DSPEC 50 offers high voltage supply flexibility having both internal HV supplies and support for ORTEC DIM and SMART-1 detector HV systems.

Internal HV Supplies

Positive Output: Rear-panel SHV connector, +500 to +5 kV. Computer controlled. Only active when the unit is set for positive bias.

Negative Output: Rear-panel SHV connector, –500 to –5 kV. Computer controlled. Only active when the unit is set for negative bias.

Shutdown In: Rear-panel BNC is used to turn off the bias supply voltage in the event that the detector warms up. The SHUTDOWN must be connected to the Bias Shutdown of the detector, or the high voltage will not turn on. The remote shutdown may be set to ORTEC or TTL mode via computer control.

In ORTEC mode, the Remote Shutdown has the following properties:

- An open circuit applied to the SHUTDOWN input indicates a warm detector; therefore, the high voltage is turned off.
- Drawing a current of 0.33 mA from the SHUTDOWN input indicates a cool detector; therefore, the high voltage can be turned on.

In TTL Mode, the Remote Shutdown has the following properties:

- An open circuit or a >2.4 V signal on the input indicates that the detector is cool.
- A <0.8 V signal on the input indicates that the detector is warm and the supply should be off.

The SHUTDOWN input is clamped at -700 mV by an internal clamp. For use with a detector without a shutdown circuit, this feature can be defeated by being left open in TTL mode.

DIM and SMART-1 Detector Types

On a SMART-1 HPGe detector, the HV module is integral with the detector itself. For “legacy” or “non-SMART-1” detectors, the HV supply is in the form of a Detector Interface Module or “DIM” with 2 m cables. The DIM has a mating connector for the traditional detector cable set: 9-pin D preamp power cable, Analog In, Shutdown In, Bias Out, and Inhibit In.

DIMS for non-SMART-1 detectors are available with the following high voltage options:

DIM-POSGE: Detector Interface Module for ANY Non-SMART-1 positive bias HPGe detector.

DIM-NEGGE: Detector Interface Module for ANY Non-SMART-1 negative bias HPGe detector.

DIM-POSNAI: Detector Interface Module for ANY positive bias NaI detector.

DIM-296: Detector Interface Module with Model 296 ScintiPack tube base/preamplifier/bias supply for NaI detectors with 14-pin, 10 stage photomultiplier tubes.

Front Panel Display: In all cases, Bias Voltage Setting and Shutdown polarity are set from the computer. The DSPEC 50 can monitor the output voltage and shutdown state; Detector high voltage value (read only); and Detector high voltage state (on/off) are displayed on the front panel LCD. The SMART-1 detector provides additional state-of-health information by monitoring the following functions: Detector element temperature (read only); Detector overload state; and Detector serial number (read only).

DSP^{EC}50/50A and DSP^{EC}502/502A

Ordering Information

- Detector connection cable not included.

| Model | Description |
|-------------|---|
| DSPEC-50 | DSPEC 50 with MAESTRO Software, single MCA, and single internal High Voltage Power Supply. |
| DSPEC-502 | DSPEC 502 with MAESTRO Software, two MCAs, and two internal High Voltage Power Supplies. |
| DSPEC-50A | DSPEC 50 (Advanced) with MAESTRO-Pro Software, single MCA, and single internal High Voltage Power Supply. |
| DSPEC-502A | DSPEC 502 (Advanced) with MAESTRO-Pro Software, two MCAs, and two internal High Voltage Power Supplies. |
| DSPEC-UPG-A | Upgrade of DSPEC-50 to DSPEC-50A or DSPEC-502 to DSPEC-502A. Requires return to factory. |

Detector Connection Cable

| | |
|---------------|--|
| 931431 | Detector Interface Module (DIM) cable, 4-ft length. |
| 683410 | Detector Interface Module (DIM) cable, 10-ft length. |
| DIM-CABLE-X-S | Detector Interface Module (DIM) cable; X=length, ft |

Specifications subject to change
062920

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